REMARKS:

This is in response to the Office Action dated September 13, 2001. Applicant amends claims 1 and 15 of the application and adds new claims 16-19. Pursuant to this amendment, claims 1-6 and 15-19 are pending in the application. Reexamination and reconsideration of the application are respectfully requested.

The Examiner rejects claims 1-4 and 15 as anticipated by Taniguchi JP 03-290623. This rejection is respectfully traversed.

The applicant amends claims 1 and 15 to add the word "driving" before the term "thin film transistors". This clarifies that the plurality of thin film transistors, "each located outside of said plurality of pixel electrodes", are driving TFTs, i.e., TFTs in the driving circuit. Consequently, these claims require the portion of the wire having a lamination structure to be "located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire". This distinguishes the claimed structure from the Taniguchi reference. The Taniguchi reference shows a shorting bar that has a multilayer construction. The shorting bar, however, is not shown to be located outside of any driving TFTs. Accordingly, claims 1-4 and 15 are patentable over the Taniguchi reference.

Newly added claims 16 and 17 depend from claim 1 and are therefore also patentable.

The Examiner rejects claim 6 as being unpatentable over U.S. Patent No. 5,671,026 to Shiraki et al. in view of "Kouchi et al., US Patent 5,886,385". The applicant respectfully submits that this rejection is detective and traverses such rejection.

First, the applicant notes that U.S. Patent No. 5,886,385 is not issued to Kouchi et al. Second, neither a Kuochi patent nor U.S. Patent No. 5,886,385 was made of record -- none is listed in any PTO-892 forms nor cited by the applicant, and no copy of this reference was furnished by the PTO. Based on section 5 of the Office Action, the applicant assumes that the Examiner intended to cite Kouchi US

5886365. Clarification is respectfully requested. Further, the Examiner is requested to list the correct identification of this reference in a PTO-892 form.

Even if the applicant assumes that Kouchi US 5886365 was the reference being cited, the applicant is still unable to determine the precise prior art teaching being relied on by the Examiner. The Examiner stated (page 4, lines 8-10 of the Office Action) that "the secondary references all show multilayer external circuits ... The terminals required a multilayer structure for passibation ...". The applicant is unable to understand this statement because only one secondary reference is cited. Kuochi US 5886365 does not appear to teach a multilayered terminal structure. The Examiner then went on to discuss Yamazaki (page 4, 4th line from the bottom), but no Yamazaki reference is identified in the heading of section 3 of the Office Action (page 3, last two lines). For these reasons, the applicant respectfully submits that the Examiner failed to clearly identify the references being relied on, and further, Kouchi U.S. Patent No. 5,886,385 does not contain the teaching relied on by the Examiner. Accordingly, the applicant submits that claim 6 is patentable.

Regarding Section 4 of the Office Action on page 5, the rejection is not clear. The section heading appears to be a repetition of the heading of section 2 (see page 2), and the paragraph under the heading of section 4 seems to be a repetition of the last paragraph of section 3 (the paragraph bridging pages 4 and 5). Therefore, the applicant is unable to determine the nature of this rejection nor to respond to the same. Clarification and/or withdrawal of this rejection is respectfully requested.

In section 5 (pages 5-6), the Examiner rejects claim 3 as being unpatentable over Kouchi et al. US 5886365 in view of Shiraki et al US 5926234. This rejection is respectfully traversed.

It appears that the Examiner's rejection is based on an incorrect understanding that claim 3 does not require the peripheral protection line to be multilayer. See page 5 of the Office Action, lines 2-3 from the bottom. The applicant respectfully disagrees. Claim 3, as amended by an amendment dated March 12, 2002, recites: "at least a portion of one of said wires having a lamination structure comprising two or more conductive layers formed of two or more layers

included in each switching thin film transistor and/or each driving thin film transistor, the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire." Further, as discussed earlier, the Kouchi reference does not appear to teach multilayer wires in the peripheral portion of the display. Accordingly, claim 3 is believed to be patentable. New claims 18 and 19 depend from claim 3 and are therefore also patentable.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6870 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: April 23, 2003

By: _____
Ying Chen
Registration No. 50,193
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701

Version with markings to show changes made:

In the claims:

1. (Thrice Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels;

a plurality of driving thin film transistors, each located outside of said plurality of pixel electrodes and comprising a plurality of conductive layers, for controlling supplying of signal voltage to the plurality of pixel electrodes;

a plurality of input terminals for receiving a control signal for the signal voltage to be supplied to the plurality of driving thin film transistors; and

wires, at least some of said wires being connected between said plurality of driving thin film transistors and said plurality of input terminals for sending the signal voltage from the plurality of input terminals to the plurality of driving thin film transistors, at least a portion of one of said wires having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the driving thin film transistors, the portion of the wire being located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire.

15. (Twice Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels;

a plurality of driving thin film transistors, each located outside of said plurality of pixel electrodes and comprising a plurality of conductive layers, for controlling supplying of signal voltage to the plurality of pixel electrodes;

a plurality of input terminals for receiving a control signal for the signal voltage to be supplied to the plurality of driving thin film transistors; and

wires, at least some of said wires being connected between said plurality of driving thin film transistors and said plurality of input terminals for sending the signal voltage from the plurality of input terminals to the plurality of driving thin film transistors, wherein each of the wires includes a first conductive layer formed of the lowest conductive layer of the driving thin film transistor and a second conductive layer situated above the first conductive layer and formed of other conductive layer of the driving thin film transistor, at least a portion of one of said wires being located near the peripheral area of the substrate and outside of said plurality of driving thin film transistors to function as an electric shielding wire.